CLAIMS

What is claimed is:

1. A method for supporting sleep mode wake up in a home phone line network, comprising the steps of:

(a) detecting a limited automatic repeat request (LARQ) header in a frame;

(b) stripping the LARQ header and a frame check sequence (FCS) in the frame;

(c) recalculating the FCS for the stripped frame; and

(d) adding the recalculated FCS to the stripped frame.

2. The method of claim 1, wherein the stripping step (b) further comprises:

(b1) placing information in the LARQ header in a frame status frame which will follow the stripped frame.

3. The method of claim 1, further comprising:

(e) sending the stripped frame with the recalculated FCS to an Ethernet controller.

4. The method of claim 3, further comprising:

(f) determining if a bit pattern at a set byte location in the stripped frame matches a wake pattern.

5. A home phone line controller, comprising:

a first logic block for detecting a LARQ header in a frame;

a second logic block for stripping the LARQ header and a FCS in the frame; and

a third logic block for recalculating the FCS for the stripped frame and for adding the recalculated FCS to the stripped frame.

6. The controller of claim 5, wherein an asserted first signal to the first logic block indicates that the LARQ header is enabled and must be stripped from the frame.

7. The controller of claim 5, wherein the first logic block asserts a second signal and a third signal to the second logic block, wherein the second signal indicates that the FCS is to be stripped from the frame, wherein the third signal indicates that the LARQ header is to be stripped from the frame.

8. The controller of claim 5, wherein an asserted fourth signal to the third logic block enables the recalculation of the FCS.

9. A system, comprising:

an Ethernet controller in a sleep mode; and

a home phone line network controller, wherein the home phone line network controller comprises:

a first logic block for detecting a LARQ header in a frame,

a second logic block for stripping the LARQ header and a FCS in the frame,

and

a third logic block for recalculating the FCS for the stripped frame and for adding the recalculated FCS to the stripped frame.

10. The system of claim 9, wherein an asserted first signal to the first logic block indicates that the LARQ header is enabled and must be stripped from the frame.

11. The system of claim 9, wherein the first logic block asserts a second signal and a third signal to the second logic block, wherein the second signal indicates that the FCS is to be stripped from the frame, wherein the third signal indicates that the LARQ header is to be stripped from the frame.

12. The system of claim 9, wherein an asserted fourth signal to the third logic block enables the recalculation of the FCS.